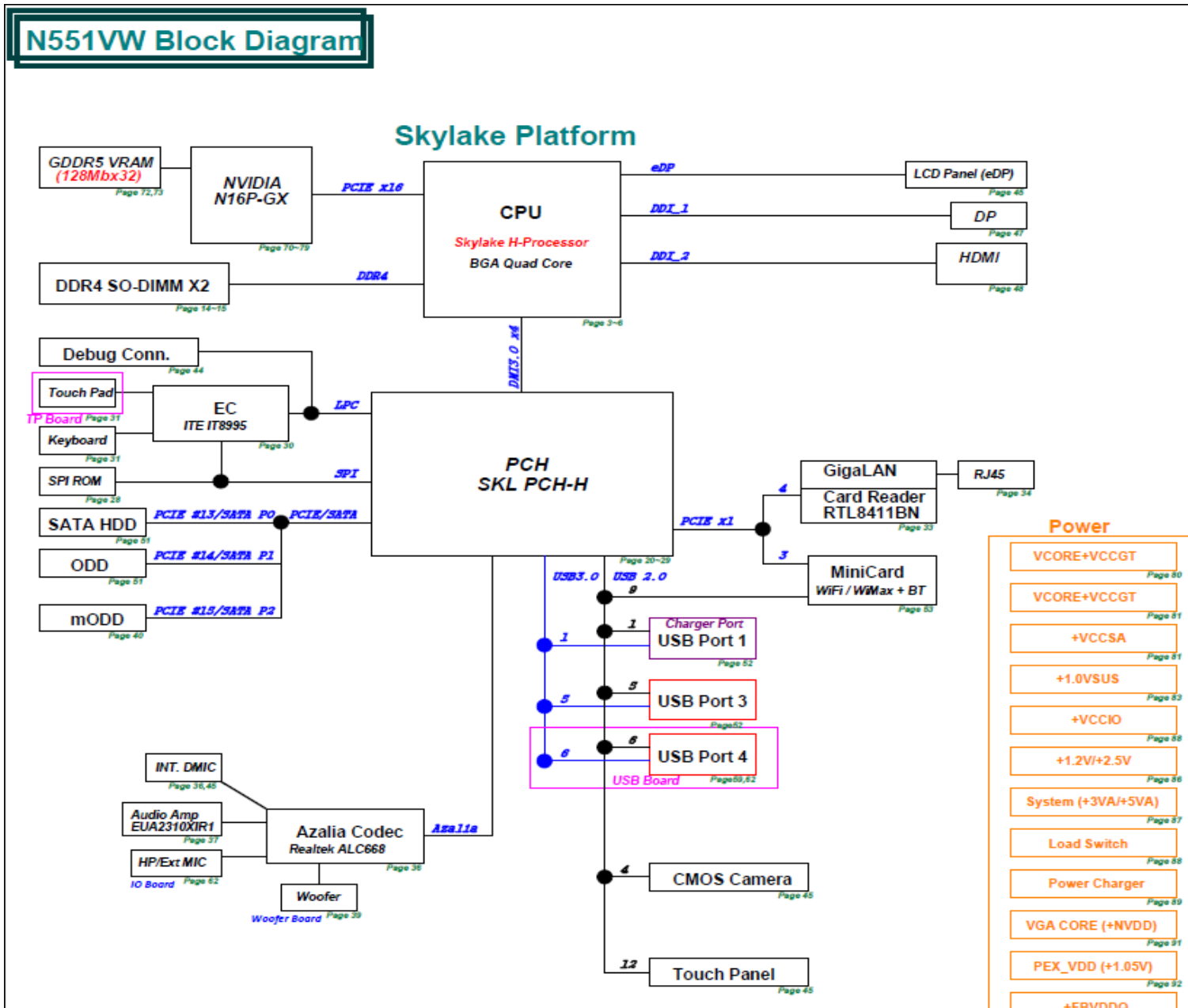
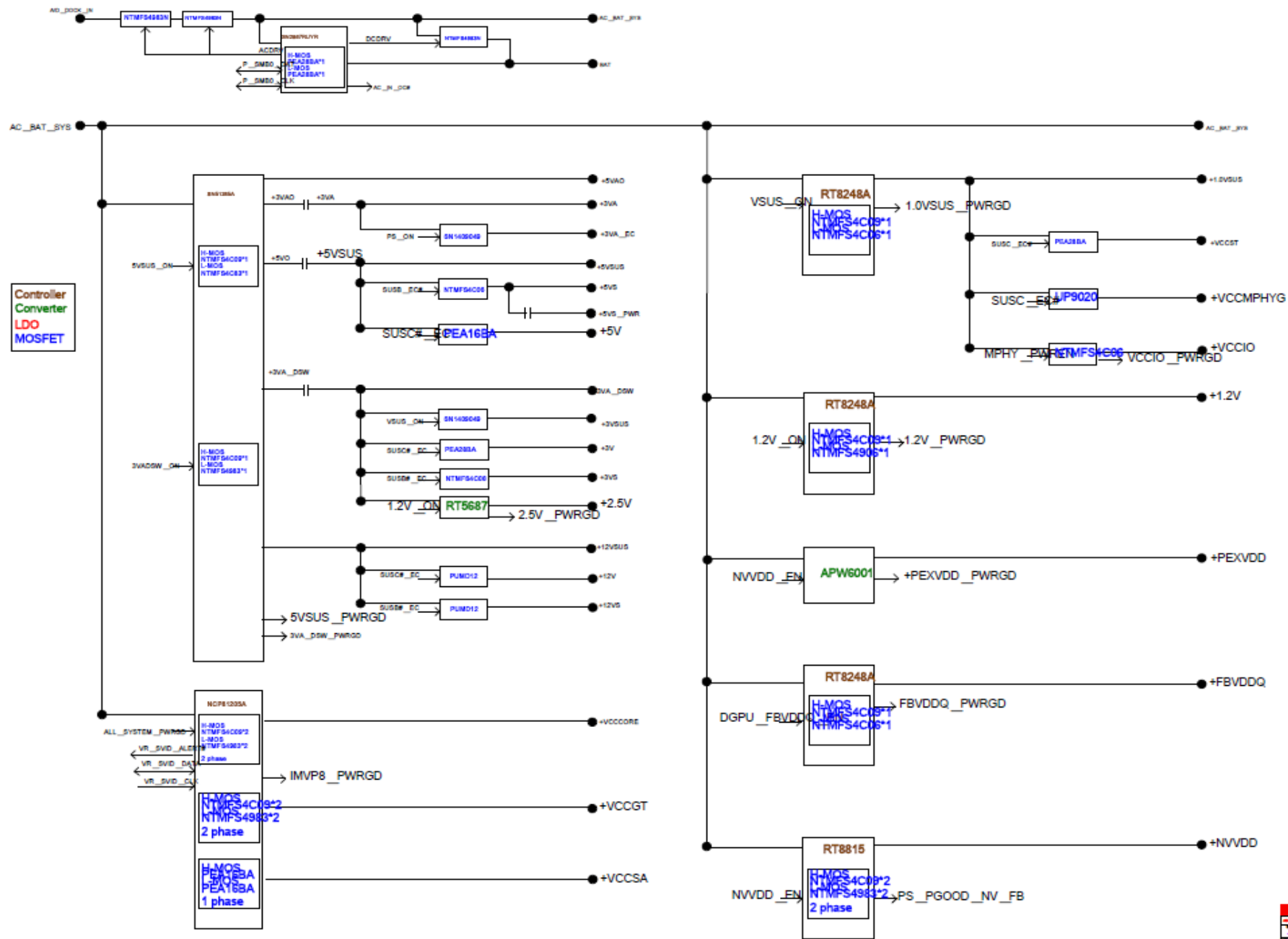


BLOCK DIAGRAM

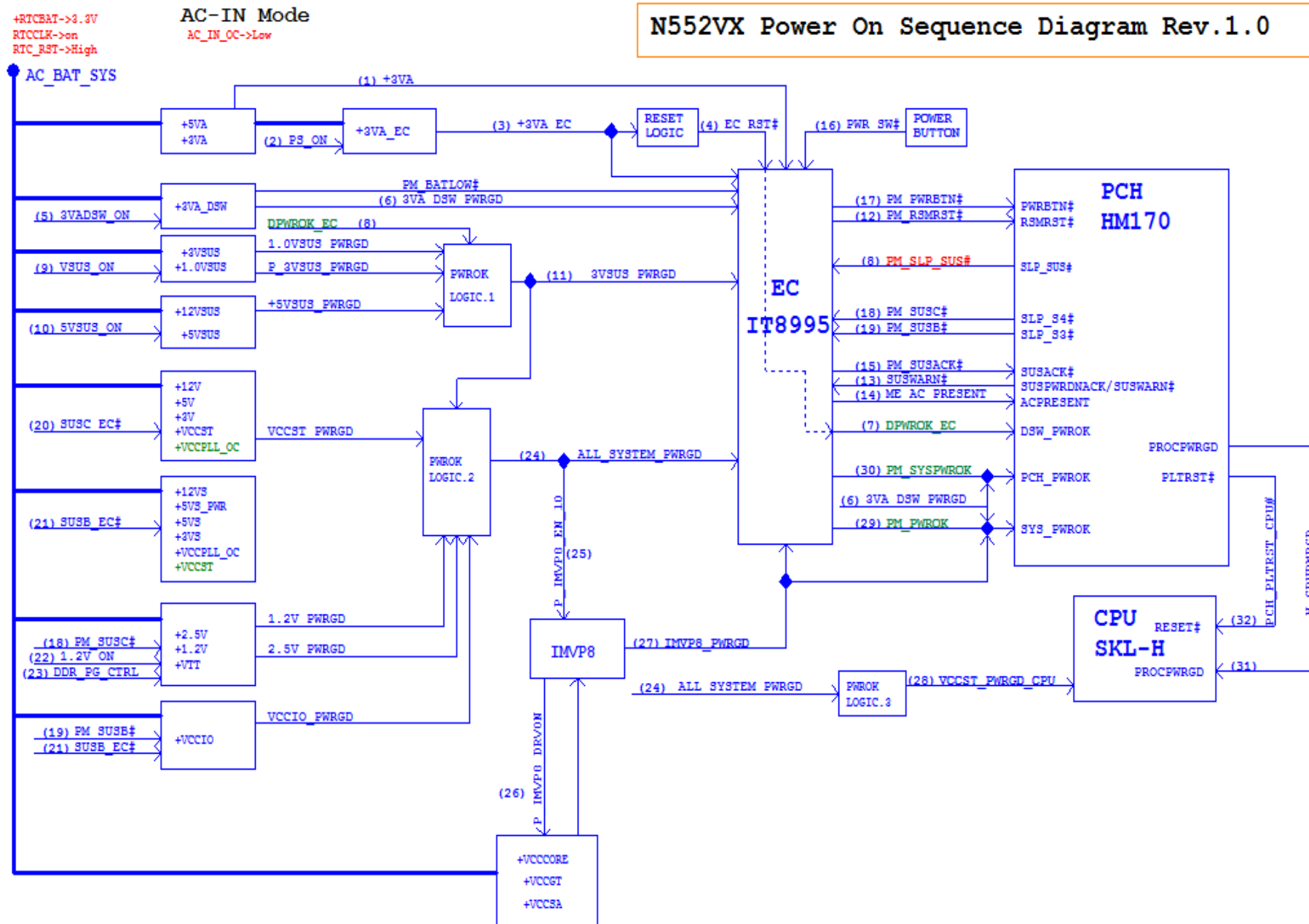


POWER FLOW



POWER ON SEQUENCE

N552VX Power On Sequence Diagram Rev.1.0



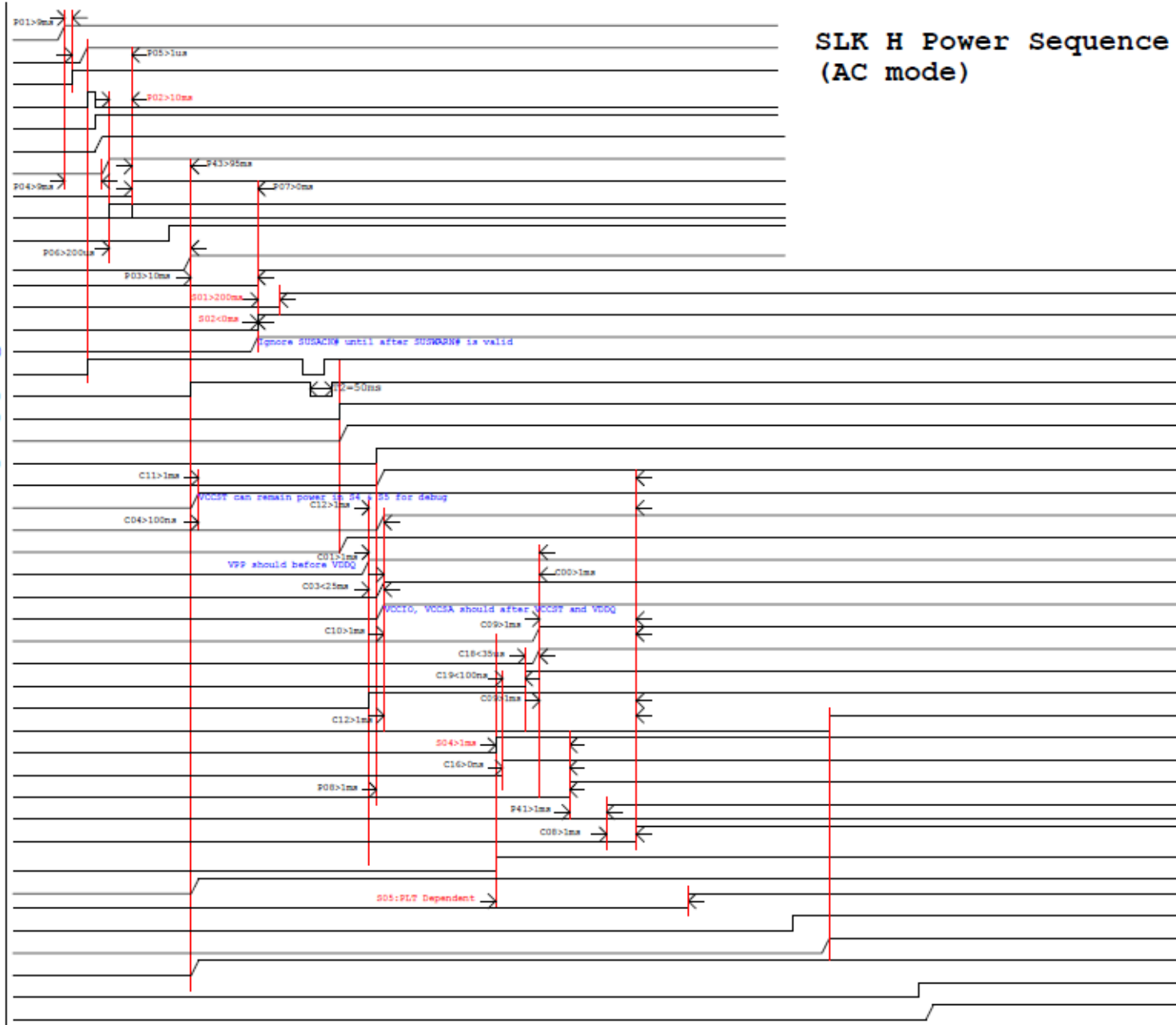
AC_IN POWER ON SEQUENCE

AC-IN Mode

```

C: CPU (+RTCRBAT)+3VA_RTC
P: PCH (AC_BAT_SYS)+3VA/+5VA
S: PLT (+3VA_RTC) RTCRST# (PCH)
Power (Power) AC_IN_OC# (EC)
Signal (EC) PS_ON (+3VA_EC)
(PB_ON)+3VA_EC (EC)
(2VADSW_ON)+3VA_DSW (3VA_DSW_FWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) EM_BATLOW# (PCH)
(PCH) EM_SLP_SUS# (EC)
(VBUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_FWRGD)
(EC) PM_R3MRST#_PCH (PCH)
(PCH) SUBWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR_Switch) PWR_SW# (EC)
(EC) PM_FWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#)+12V/+5V/+3V
(EC) SUBS_EC# (Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(VBUS_ON)+1.0V_VCCST,VCCPLL (VCCST_FWRGD)
(+VCCIO)+VCCSTG
(1.2V_ON)+2.5V (2.5V_FWRGD)
(1.2V_ON)+VDDQ_CPU (1.2V_FWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO (VCCIO_FWRGD)
(ALL_SYSTEM_FWRGD)+VCCSA (IMVP8_FWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_FWRGD (AND)
(Power) IMVP8_FWRGD
(AND) ALL_SYSTEM_FWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_FWRGD) VCCST_FWRGD_CPU (CPU)
(EC) PM_FWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUFWRGD (CPU)
(ALL_SYSTEM_FWRGD) P_IMVP8_EN_I0 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE (IMVP8_FWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCCG

```



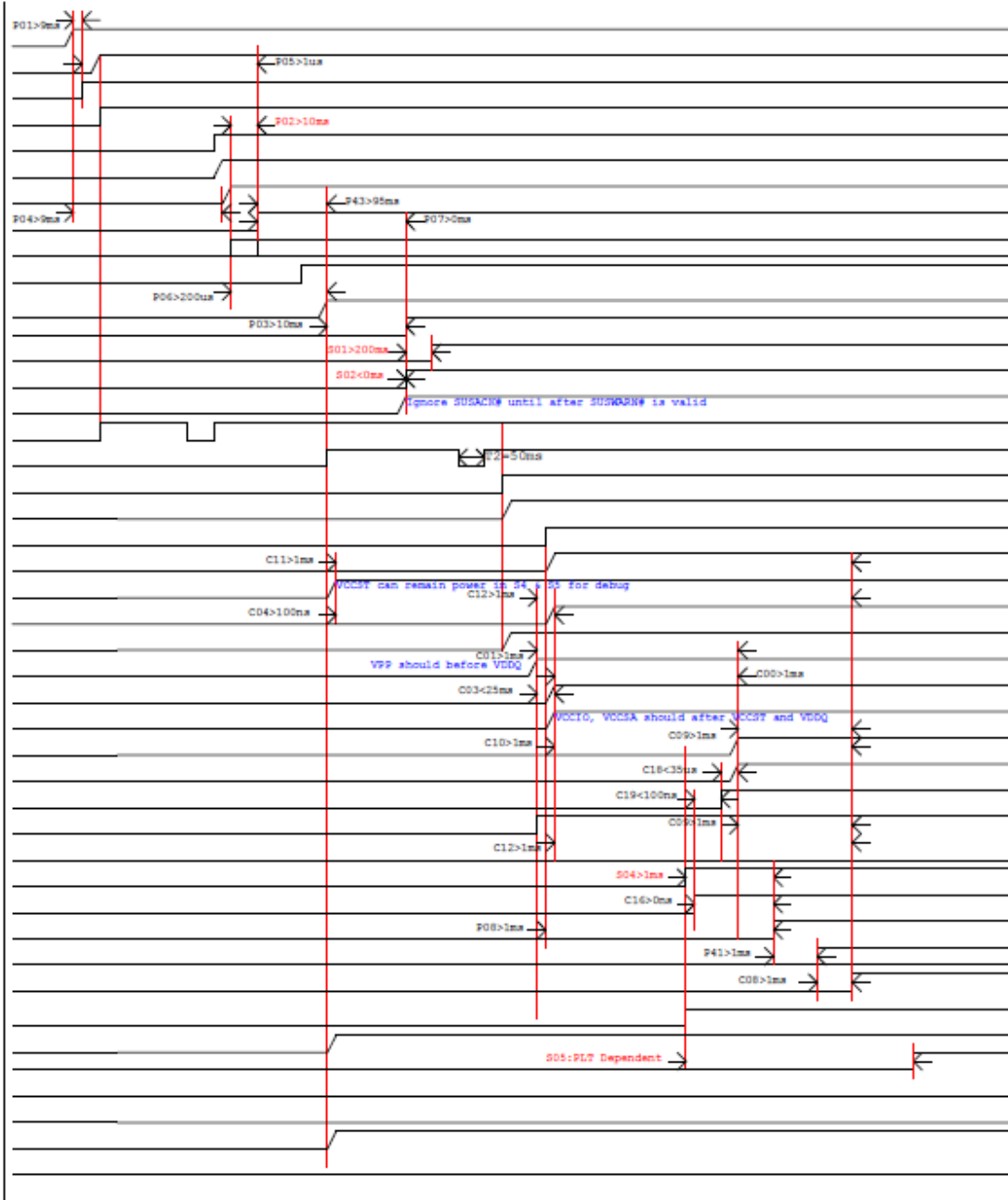
SLK H Power Sequence (AC mode)

DC_IN POWER ON SEQUENCE

DC-IN Mode

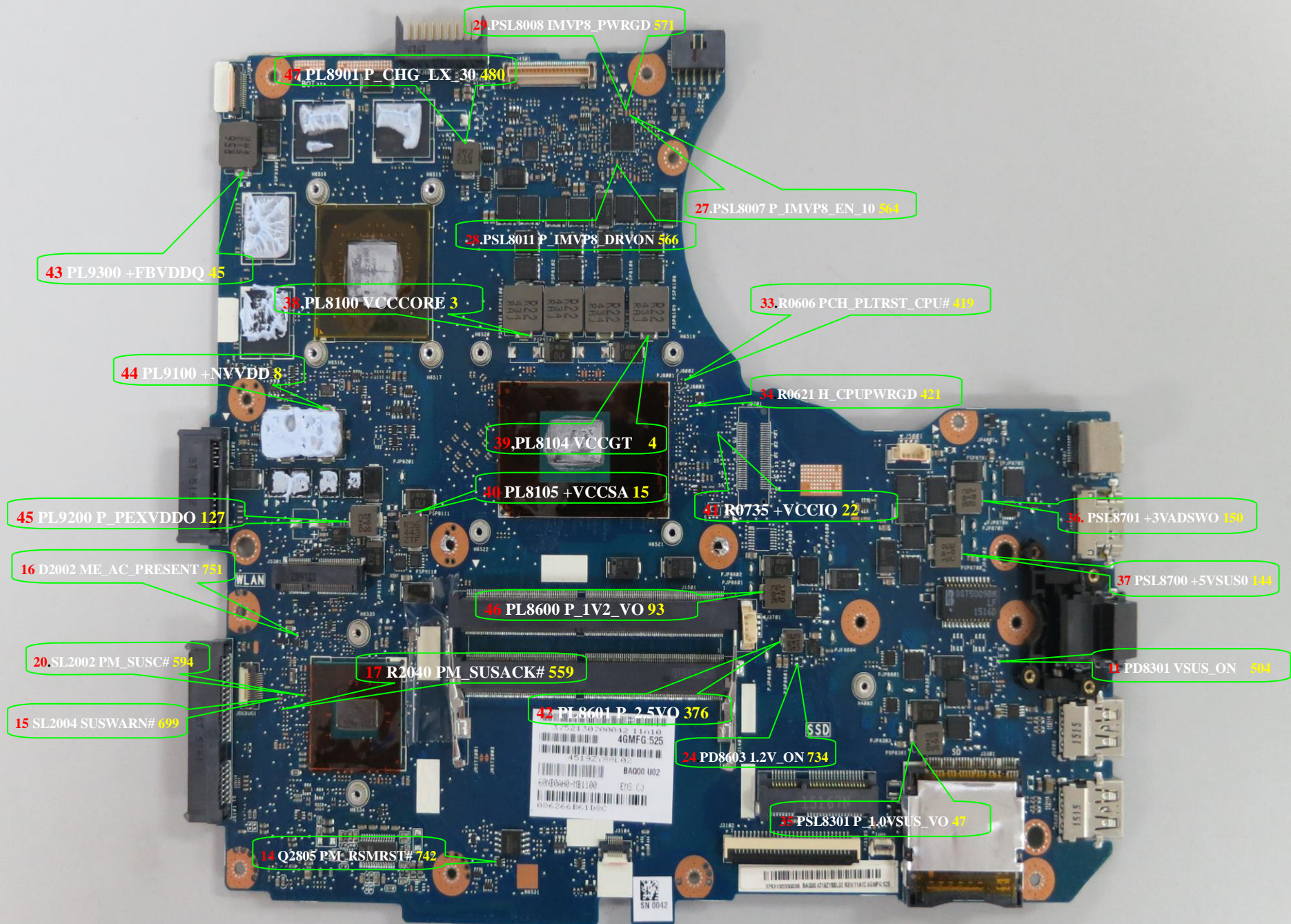
C: CPU
 P: PCH
 S: PLT
 Power
 Signal

(+RTCBAT) +3VA_RTC
 (AC_BAT_SYS) +3VA/+5VA
 (+3VA_RTC) RTCRST# (PCH)
 (Power) AC_IN_OC# (EC)
 (EC) PS_ON (+3VA_EC)
 (PS_ON) +3VA_EC (EC)
 (3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
 (EC) DPWR0K_EC (PCH)
 (+3VA_DSW) PM_BATLOW# (PCH)
 (PCH) PM_SLP_SUS# (EC)
 (VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
 (EC) PM_RSMRST#_PCH (PCH)
 (PCH) SUSWRN# (EC)
 (EC) ME_AC_PRESENT_PCH (PCH)
 (EC) PCH_SUSACK# (PCH)
 (PWR_Switch) PWR_SW# (EC)
 (EC) PM_PWRBTN# (PCH)
 (EC) SUSC_EC# (Power)
 (SUSC_EC#) +12V/+5V/+3V
 (EC) SUBS_EC# (Power)
 (SUBS_EC#) +12VS/+5VS/+3VS
 (VSUS_ON) +1.0V_VCCST, VCCPLL (VCCST_PWRGD)
 (+VCCIO) +VCCSTG
 (1.2V_ON) +2.5V (2.5V_PWRGD)
 (1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
 (+12VS) +VCCPLL_OC
 (SUBS_EC#) +VCCIO (VCCIO_PWRGD)
 (ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
 (DDR_VTT_CTRL) +0.6V
 (CPU) DDR_VTT_CTRL (Power)
 (Power) 1.2V_PWRGD (AND)
 (Power) IMVP8_PWRGD
 (AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
 (ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
 (EC) PM_PWR0K_PCH (PCH)
 (PCH) CLK_PCH_BCLK (CPU)
 (PCH) H_CPU_PWRGD (CPU)
 (ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
 (CPU) P_SVID_DATA_X2 (Power)
 (EC) PM_SYSFWR0K_PCH (PCH)
 (PCH) PLT_RST# (CPU/EC/Device)
 (P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
 (CPU) H_THERMTRIP# (PCH)
 (PCH) DDR4_DRAMRST# (Memory)
 +VCCGT



SLK H Power Sequence (DC mode)

Signal Measure Point-Bottom



Signal Measure Point-Top

